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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/643,283 | 08/18/2003 | Gregory A. Uvieghara | 020716 | 4076 |

23696 7590 05/19/2004

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| EXAMINER | |
|---|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/643,283 | UVIEGHARA, GREGORY A. | |
| | Examiner | Art Unit | |
| | Kenneth B. Wells | 2816 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,13,29 and 30* is/are rejected.

7)☒ Claim(s) *5-12, 14-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The disclosure is objected to because of the following informalities: on page 3, line 14, "complementary" is misspelled (note also claim 7, line 2). On page 3, line 20, "mechanism further includes" is grammatically improper. On page 6, line 5, --the-- should be inserted after "from". On line 19 of page 6, --T8-- should be inserted after the word "transistor". On page 12, line 20, "84" should be changed to --94--. On page 14, the fourth line from the bottom, "10" should be changed to --110--. On page 15, line 3, "have also" should be changed to --also have--. On the second to last line of page 17, "the" is misspelled. On page 18, line 16, "130 the latch 110" is grammatically improper, as is "state represented Vdd" on line 24 of page 18. On page 19, line 6, "132" appears to be incorrect, and on the last line of page 19, "Accordingly" should be deleted.

3. The drawings are objected to because in Fig. 4, reference numeral 82 should be pointing to a MUX (not to the signal line connected between the output of pass gates 126, 128 and the gate

terminal of FET T6). Also in Fig. 4, te additional logic 112 reference numeral is not pointing to NAND gate 122, and thus is inconsistent with the specification at page 15, line 14. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The claims are objected to because of the following informalities: in claim 1, line 1, "a" should be changed to --an integrated--(note also line 1 of claim 9). In claim 2, "said first circuit" and "said second circuit" should be changed to --said first circuit component--and --said second circuit component--, respectively (note also that claim 30 needs the same change). In claim 8, line 1, "said feedback path" lacks antecedent basis. In claim 10, line 2, "leakage paths" lacks clear antecedent basis because a leakage path has already been recited (e.g., see claim 1) and thus claim 10 should recite "additional leakage paths" if this is in fact what applicant means in claim 9. The same type of problem exists for "any remaining unblocked leakage paths" in claim 11, "means for blocking said path" in claim 12 (see claim 1, line 3), "means for blocking leakage paths" in claim 14, line 3, etc. In claim

20, "said data path" lacks antecedent basis. Also note that "said master cell" in claim 10 lacks antecedent basis.

5. Claim 29 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase "via one or more of said HVT transistors" is vague and indefinite, i.e., it cannot be determined what is meant by reciting that the leakage paths through the LVT transistors are blocked "via" the HVT transistors. Where is this supported in the drawings and specification?

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 13 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Chappell et al.

Note Fig. 8, where the recited "electrical path" reads on the current path from the power supply terminal, through FET

QS3, Q2 and FET QS4 to ground; the recited blocking means reads on the combination of FETs QS3 and inverter 82 (which are part of a feedback path within the IC of Fig. 8); the recited first and second circuit components" read on FETs QS3 and inverter 82; the recited "means for preserving data" reads on the half latch formed by FET QS3 and inverter 82; and the limitation of claim 4 is met by the discussion of the "stand-by" state/mode (see column 7, line 64). In Fig. 8 of Chappell et al, when the input to inverter 82 is logic "0", its output is logic "1" and so QS3 is cutoff, which block the above-noted current path.

As an alternative interpretation of Fig. 8, there is a feedback signal from NAND gate 87 to the input of FET Q23 which performs current path blocking; the first and second circuit components read on the combination of FETs Q23, Q25, Q26 and NAND gate 87, respectively; the path is from the high power supply terminal through FETs Q23, Q25 and Q26 down to ground (it is cutoff when the output of NAND gate 87 goes high).

Also note that the clock signal recited in claim 13 can be read on any of the three clock signals shown in Fig. 8 of Chappell et al.

7. Claim 29 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Claims 5-12 and 14-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Note Fig. 2 of Hsu et al.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth B. Wells
Primary Examiner
Art Unit 2816

May 14, 2004